What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

memory cells which can be electrically programmed and each of which has at least three storage states;

a memory cell array constituted by said plurality of memory cells arranged in a matrix;

a plurality of data circuits for temporarily storing data for controlling write operation states of said plurality of memory cells in said memory cell array;

write means for performing a write operation to said plurality of memory cells in accordance with contents of said data circuits respectively corresponding to said plurality of memory cells;

write verify means for checking states of said plurality of memory cells set upon the write operation; and

data circuit content updating means for updating the contents of said data circuits such that a rewrite operation is performed to only a memory cell, in which data is not sufficiently written, on the basis of the contents of said data circuits and the states of said memory cells set upon the write operation;

wherein the write operation and a write verify operation based on the contents of said data circuits, and an operation for updating the contents of said data circuits are repeatedly performed until said

plurality of memory cells are set in predetermined written states, thereby electrically performing a data write operation.

2. A nonvolatile semiconductor memory device comprising:

a memory cell array constituted by a plurality of memory cells which are arranged in a matrix and each of which can be electrically programmed,

each of said memory cells having at least three storage states and storing arbitrary data "i" ($i = 0, 1, \ldots, n - 1$; $n \geq 3$) as multivalue data, and a storage state corresponding to data "0" being an erasure state;

a plurality of data circuits each serving as a sense amplifier and having a function of sensing data and a function of storing sensed information as data for controlling a write operation state of a corresponding memory cell in said memory cell array;

write means for performing a write operation to said plurality of memory cells in accordance with contents of said data circuits respectively corresponding to said plurality of memory cells;

ith ($i = 1, 2, \ldots, n - 1$) write verify means for checking whether the storage state of each of said plurality of memory cells set upon the write operation becomes a storage state of data "i";

ith ($i = 1, 2, \ldots, n - 1$) data circuit content

simultaneous updating means, said data circuit content simultaneous updating means for simultaneously updating the contents of data circuits corresponding to a memory cell in which data "i" is to be stored, such that a rewrite operation is performed to only a memory cell, in which data is not sufficiently written, on the basis of the contents of said data circuits and the storage states of said memory cells set upon the write operation; and

data circuit content updating means for performing a storage checking operation performed by said ith write verify means and a simultaneously updating operation performed by said ith data circuit content simultaneous updating means to data "1" to data "n - 1" n - 1 times to update the contents of all said data circuits,

wherein said ith data circuit content simultaneous updating means, of bit line potentials at which the storage states of said memory cells set upon a write operation are output by said ith write verify means, corrects in accordance with the content of said data circuits, senses/stores, as rewrite data, a bit line potential corresponding to a memory cell in which data "i" ($i \geq 1$) is to be stored, updates the contents of said data circuits, corrects the bit line potential at which the state of said memory cell set upon the write operation is output in accordance with the contents of said data circuits such that bit line potentials

corresponding to memory cells in which data except for data "i" are to be stored are sensed/stored such that the contents of said data circuits are held, holds the data storage states of said data circuits until the bit line potentials are corrected, operates said data circuits as sense amplifiers while the corrected bit line potentials are held, and updates simultaneously the contents of said data circuit corresponding to said memory cell in which data "i" is to be stored,

a write operation based on the contents of said data circuits and a data circuit content updating operation are repeatedly performed until said plurality of memory cells are set in predetermined written states, thereby electrically performing a data write operation.

3. A device according to claim 2, wherein a data circuit content simultaneous updating operation based on the contents of said data circuits can simultaneously update data with respect to a plurality of bit lines of said memory cell array.

4. A device according to claim 3, wherein said data circuits control write operation states of said memory cells in accordance with data stored in said data circuits in a write operation to perform control such that the states of said memory cells are changed into predetermined written states or the states of said memory cells are held in states set prior to the write

operation,

for a data circuit corresponding to a memory cell to be set in an "i"-data-written state, said ith data circuit content simultaneous updating means,

changes data of said data circuit into data for controlling the state of said memory cell to hold the state of said memory cell in a state set prior to the write operation when a memory cell corresponding to a data circuit in which data for changing a memory cell into the "i"-data-written state reaches a predetermined written state,

sets data for controlling the state of said memory cell to change the state of said memory cell into the "i"-data-written state in said data circuit when a memory cell corresponding to a data circuit in which data for changing a memory cell into the "i"-data-written state does not reach a predetermined written state, and

for the data circuit that data for controlling the state of said memory cell to hold the state of said memory cell in a state set prior to the write operation is stored, sets data for controlling the state of said memory cell to hold the state of said memory cell in a state set prior to the write operation in said data circuit, and

said ith data circuit content simultaneous updating means does not change contents of said data circuits

corresponding to said memory cells in which data except for the "i" are to be stored.

5. A device according to claim 4, wherein each of said memory cells is constituted by stacking and forming a charge accumulation layer and a control gate on a semiconductor layer and stores arbitrary data "i" ($i = 0, 1, \ldots, n - 1; n \geq 3$) as at least three storage stages and as multivalue data using magnitudes of threshold voltages, and

said ith write verify means applies a predetermined ith verify potential to said control gate to read out and check whether a threshold voltage of a memory cell set to be the "i"-data-written state is a desired threshold voltage.

6. A device according to claim 5, wherein a storage state corresponding to data "0" is an erased state, a difference between a threshold voltage corresponding to the data "n - 1" state and the threshold voltage corresponding to a data "0" state is maximum, and threshold voltages corresponding to data "1", "2",..., "i",..., "n - 2" states range from the threshold voltage corresponding to the data "0" state to the threshold voltage corresponding to the data "n - 1" state, and

the threshold voltages corresponding to the data "1", "2",..., "i",..., "n - 2" states are ordered from the threshold voltage corresponding to the data "0" state,

said device further comprises

a first bit line potential setting circuit for, of a plurality of bit line potentials at which states of memory cells set upon a write operation are output by said ith write verify means, when said data circuits sense a bit line potential corresponding to a data circuit whose contents are data for controlling the states of said memory cells to hold the states of said memory cells in states set prior to the write operation, setting a bit line potential to be a first correction bit line potential for obtaining data for controlling the states of said memory cells to hold states of said memory cells in states set prior to the write operation, and

a jth bit line potential setting circuit for, of bit line potentials corresponding to memory cells set to be data "j"-written states ($i + 1 \leq j$) among bit line potentials at which states of said memory cells set upon a write operation are output by said ith ($1 \leq i \leq n - 2$) write verify means, when a data circuit senses only a bit line potential corresponding to a data circuit whose contents are data for controlling states of memory cells to set the states of said memory cells in data "j"-written states, setting the bit line potential in a second correction bit line potential for obtaining data for controlling the states of said memory cells to change the states of said memory cells into the data

"j"-written states,

wherein, to update the contents of said data circuits, a bit line potential at which states of said memory cells set upon a write operation are output by an ith write verify operation is corrected by said first, (i + 1)th, (i + 2)th,..., (n - 1)th bit line potential setting circuits.

7. A device according to claim 6, wherein each of said data circuits is constituted by a first data storage unit for storing information indicating whether a state of a memory cell is held in a state set prior to a write operation and a second data storage unit for, when the information of said first data storage unit is not information for controlling the state of said memory cell to hold the state of said memory cell in a state set prior to the write operation, storing information indicating a written state "i" (i = 1, 2,..., n - 1) to be stored in said memory cell,

said first data storage unit having a function of sensing/storing bit line potentials which are corrected by said first, (i + 1)th, (i + 2)th,..., (n - 1)th bit line potential setting circuits in accordance with the contents of said data circuits to perform the data circuit content updating operation and at which the storage states of said memory cells set upon the write operation are output by the ith write verify operation.

8. A device according to claim 7, further

comprising:

a write prevention bit line voltage output circuit for, when the information of said first data storage unit is information for controlling the state of said memory cells to hold the state of said memory cells in states set prior to a write operation, outputting a write prevention bit line voltage to a bit line in the write operation; and

an ith (i = 1, 2,..., n - 1) bit line voltage output circuit for, when the information of said first data storage unit is not information for controlling the states of said memory cells to hold the states of said memory cells in the states set prior to the write operation, outputting an ith bit line voltage in the write operation in accordance with information of said second data storage unit indicating a written state "i" to be stored in a memory cell.

9. A nonvolatile semiconductor memory device comprising:

memory cells which can be electrically programmed;

a memory cell array constituted by said plurality of memory cells arranged in a matrix;

threshold voltage detection means for charging a bit line connected to said memory cells through said memory cells; and

a sense amplifier for sensing a potential of said bit line charged by said threshold voltage detection

means,

wherein a bit line potential obtained by said threshold voltage detection means is determined by the threshold voltages of said memory cells.

10. A device according to claim 9, wherein each of said memory cells can be electrically programmed to store at least three data each at a different threshold voltage of said memory cell as multivalue data,

said threshold voltage detection means outputs the multivalue data of said memory cell to said bit line as a potential having multivalue levels; and

said sense amplifier senses a bit line potential having the multivalue levels.

11. A device according to claim 9, wherein said memory cells are connected in series with each other as units each constituted by a plurality of memory cells to form a plurality of NAND-cell structures, one terminal of each of said NAND-cell structure being connected to said bit line through a first selection gate, and the other terminal of each of said NAND-cell structures being connected to a source line through a second selection gate,

said threshold voltage detection means transfers a source line voltage to said bit line through a corresponding NAND cell to charge said bit line, and

non-selected control gate voltages and first and second selection gate voltages are controlled such that

voltage transfer capabilities of non-selected memory cells and first and second selection transistors are sufficiently increased to such a level that the bit line voltage is only determined by the threshold voltage of the selected memory cell.

12. A device according to claim 10, wherein said memory cells are connected in series with each other as units each constituted by a plurality of memory cells to form a plurality of NAND-cell structures each having one terminal connected to said bit line through a first selection gate and the other terminal connected to a source line through a second selection gate,

said threshold voltage detection means transfers a source line voltage to said bit line through a corresponding NAND cell to charge said bit line, and

non-selected control gate voltages and first and second selection gate voltages are controlled such that voltage transfer capabilities of non-selected memory cells and first and second selection transistors are sufficiently increased to such a level that the bit line voltage is only determined by the threshold voltage of the selected memory cell.

13. A device according to claim 10, further comprising:

a plurality of data circuits each functioning as said sense amplifier and having a function of storing

sensed information as data for controlling write operation states of said memory cells;

write means for performing a write operation in accordance with contents of said data circuits respectively corresponding to said plurality of memory cells in said memory cell array;

write verify means which uses said threshold voltage detection means to check whether states of said plurality of memory cells set upon the write operation are storage states of desired data; and

data circuit content simultaneous updating means for simultaneously updating the contents of said data circuits with respect to a plurality of bit lines such that a rewrite operation is performed to only a memory cell, in which data is not sufficiently written, on the basis of the contents of said data circuits and the states of said memory cells after write operation,

wherein said data circuit content simultaneous updating means corrects a bit line potential at which the storage states of said memory cells set upon the write operation are output, in accordance with the contents of said data circuits to sense/store the bit line potential as rewrite data, holds the data storage states of said data circuits until the bit line potential is corrected, operates said data circuits as sense amplifiers while the corrected bit line potential is held, and simultaneously updates the contents of said

data circuits, and

a write operation based on the contents of said data circuits and a data circuit content simultaneous updating operation are repeatedly performed until said memory cells are set in predetermined written states, thereby electrically performing a write operation.

14. A device according to claim 13, wherein said data circuits control write operation states of said memory cells in accordance with data stored in said data circuits in a write operation to perform control such that the states of said memory cells are changed into predetermined written states or the states of said memory cells are held in states set prior to the write operation,

said data circuit content simultaneous updating means,

changes data of said data circuits into data for holding the states of said memory cells in states set prior to the write operation when a memory cell corresponding to a data circuit in which data for controlling said memory cells to change said memory cells to have predetermined written states is stored reaches a predetermined written state,

sets data for controlling said memory cells to change said memory cells to have predetermined written states in said data circuits when said memory cell corresponding to said data circuit in which data for

controlling said memory cells to change said memory cells to have predetermined written states is stored does not reach the predetermined written state, and

sets data for controlling the states of said memory cells to hold the states of said memory cells in the states set prior to the write operation in said data circuits, when data for controlling the states of said memory cells to hold the states of said memory cells in the states set prior to the write operation is stored in said data circuits.

15. A device according to claim 14, further comprising a bit line potential setting circuit for, when, of bit line potentials at which states of said memory cells set upon the write operation are output by said threshold voltage detection means, only a bit line potential corresponding to said data circuits whose contents are data for controlling the states of said memory cells to hold the states of said memory cells in the states set prior to the write operation is sensed by said data circuits, setting a correction bit line potential at which data for controlling the states of said memory cells to hold the states of said memory cells in the states set prior to the write operation is obtained, and

wherein, to perform the data circuit content simultaneous updating operation, a bit line potential at which the states of said memory cells set upon the write

operation are output by said threshold voltage detection means is corrected by said bit line potential setting circuit in accordance with the contents of said data circuits.

16. A device according to claim 15, wherein said device is a nonvolatile semiconductor memory device in which one of said memory cells has at least three storage data "i" (i = 0, 1,..., n - 1) to perform a multivalue storing operation, a storage state corresponding to data "0" being an erased state,

each of said data circuits is constituted by a first data storage unit for storing information indicating whether a state of a memory cell is held in a state set prior to a write operation and a second data storage unit for, when the information of said first data storage unit is not information for controlling the state of said memory cell such that the state of said memory cell is held in a state set prior to the write operation, storing information indicating a written state "i" (i = 1, 2,..., n - 1) to be stored in said memory cell,

said first data storage unit having a function of sensing/storing bit line potentials which are corrected by said bit line potential setting circuits in accordance with the contents of said data circuits to perform the data circuit content updating operation and at which the storage states of said memory cells set upon the

write operation are output by the threshold voltage detection means.

17. A device according to claim 16, wherein said first data storage unit has a function of comparing a reference voltage with a bit line voltage to sense a bit line potential and

a function of sensing/storing a bit line potential which is corrected by said bit line potential setting circuit in accordance with the contents of said data circuits using a reference voltage corresponding to the contents of said data circuits and at which states of said memory cells set upon the write operation are output by said threshold voltage detection means.